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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/044,365	01/11/2002	Xiaobao Wang	015114-054910US	8233	
26059	7590 01/14/2004		EXAMINER		
	O AND TOWNSEND	CHANG, DANIEL D			
TWO EMBAI 8TH FLOOR	RCADERO CENTER	ART UNIT	PAPER NUMBER		
·	ISCO, CA 94111-3834	4	2819		
			DATE MAILED: 01/14/200	4	

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. Applicanties Office Action Summary Examiner Art Unit 2819 Examiner Daniel D. Chang Art Unit 2819 A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAIL/ING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.18(8). In no event, however, may a reply be timely filled with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAIL/ING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.18(8). In no event, however, may a reply be timely filled with 52 Ke, 100 MONTH from the maining date of this communication, which will be substant minimum of the 100 Ke) (100 Ke) and the 100 Ke) (100 Ke)				an
Examiner		Applicat	ion No.	Applicant(s)
Daniel D. Chang 2819 — The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Exherence for the remy by be included under the problemation of 3° CPR 1.136(s). In no event, however, may a reply be simply blad Exherence for the remy by the problemation of 3° CPR 1.136(s). In no event, however, may a reply be simply blad The period for reply a specified above is was than thinty (30) days, a reply within the statutory mornium of thinty (30) days and its period (s) in MOTHS from the mailing date of this communication (reply is appendix dows, the manumal estations period will apply and its epriod (s) in MOTHS from the mailing date of this communication (reply is appendix dows, the manumal reply of the communication, even if timely field, may reduce all the communication of the communication of the date of this communication (s) field on 06 October 2003. 2.2 ☐ This action is FINAL. 2.2 ☐ This action is non-final. 3.3 ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Exparte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4.1 ☐ Claim(s)		10/044,3	365	WANG ET AL.
Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Education of time may be available used the provision of 3° CFR 1.13(s), in no event, however, may a reply be limitly filled after SIX (8) MONTH(S from the mailing date of this communication, early viellant new states and the mailing date of this communication of 3° CFR 1.13(s), in no event, however, may a reply be limitly filled after SIX (8) MONTH(S from the mailing date of this communication, early viellant her benefit on the property of the mailing date of the scanner of the mailing date of the communication of the property viellant her benefit of the property of the mailing date of the communication, even if timely filled any reduce any seared potent term adjustment. See 3° CFR 1.74(t)) Status 1)∑ Responsive to communication(s) filed on 96 October 2002 2a) This action is FINAL. 2b)∑ This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4)∑ Claim(s) 1-6 and 8-28 is/are pending in the application. 4a) Of the above claim(s) is/are allowed. 6b)∑ Claim(s) 1-6 and 8-28 is/are rejected. 7) Claim(s) is/are allowed. 6b)∑ Claim(s) is/are objected to. 8) Claim(s) 1-6.8-28 is/are rejected. Application Papers 9) The drawing(s) filed on is/are: all accepted or bl_ objected to by the Examiner. Application Papers 10) The drawing(s) filed on is/are: all accepted or bl_ objected to by the Examiner. Application Papers 11 proposed drawing correction filed on is/are: all accepted or bl_ objected to by the Examiner. 12 The drawing(s) filed on is/are: all accepted or bl_ objected to by the Examiner. 13 all proposed drawing correction filed on is/are: all accepted or bl_ objected to by the Examiner. 14 proved drawing some *c Monte of *claim for foreign priority under 35 U.S.C. § 119(a	Office Action Summary	Examine	r	Art Unit
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Acknowledgement

Receipt is acknowledged of the Amendment filed October 6, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 8-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (US 4,719,369) in view of Choe et al. (US 5,721,548).

Regarding claims 1 and 2, in figures 1 and 2, Asano teaches an integrated circuit comprising:

a first transistor (20 or 21) coupled to an off-chip resistor (22 or 23, col. 4, lines 7+); an analog-to-digital converter (30) coupled to the first transistor;

a digital encoder circuit (31) coupled to receive output signals of the analog-to-digital converter; and

an impedance matching circuit (2-5, 7-10, 12-19) coupled to receive output signals of the digital encoder circuit, wherein the impedance matching circuit comprises a plurality of second transistors (2-5, 7-10) coupled in parallel.

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Asano does not specifically teaches that the analog-to-digital converter comprises comparators that compare a voltage at a terminal of the first transistor to a series of resistance values.

Choe teaches, in figure 1 (and/or 5) an analog-to-digital converter having comparators 20, and a string of resistors 10, for comparing a plurality of reference voltage with an analog input signal voltage Va and generates sets of HIGH or LOW output signals (col. 1, lines 12+)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the output circuit of Asano with the analog-to-digital circuit as taught by Choe. It is an obvious matter of substitution of equivalence or design choice.

Regarding claim 3, in figures 1 and 2, Asano shows that the impedance matching circuit is coupled in parallel (2-5, 7-10) with an I/O pin (a common output node between transistors 5 and 10) of the integrated circuit.

Regarding claim 4, in figures 1 and 2, Asano shows that the impedance matching circuit is coupled in series (from VDD or GND to I/O pin) with an I/O pin (a common output node between transistors 5 and 10) of the integrated circuit.

Regarding claim 5, in figures 1 and 2, Asano shows that the impedance matching circuit is coupled to a buffer circuit (1, 6, 11) that is coupled to the I/O pin.

Regarding claim 6, in figures 1 and 2, Asano shows a plurality of impedance matching circuits (1st impedance matching circuit 2-5, 12-15; and 2nd impedance matching circuit 7-10, 16-19) coupled to receive output signals (26, 27) of the digital encoder circuit (a combination of 31 in 24 and 25), wherein the plurality of impedance matching circuits each comprises a plurality of transistors coupled in parallel (2-5 and 7-10).

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Regarding claims 8, in figure 1 (and/or 5), Choe shows that the analog-to-digital converter comprises a plurality of resistors (10) that set threshold voltages for the plurality of comparators (20).

Regarding claims 9 and 10, in figures 1 and 2, Asano shows that the plurality of second transistors of the impedance matching circuit comprises four (2-5) or five (1-5) transistors coupled in parallel.

Method claims 11-20 are essentially the same in scope as apparatus claims 1-6 and 8-10 and are rejected similarly. Also claims 21-28 are rejected similarly.

Regarding claims 15 and 26, Asano or Choe does not show an encoder with NAND and NOR gates. However, a conventional encoder comprises NAND and NOR gates. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the encoder of Asano or Choe with an encoder with NAND and NOR gates. It is an obvious matter of design choice.

Claims 21-28 are rejected similarly with claims 1-10. Regarding the limitation, "programmable logic circuitry" in claim 21, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Daniel D. Chang Primary Examiner Art Unit 2819

DC January 8, 2004

